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Page 2 of 12**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-21. (Canceled without prejudice or disclaimer)

22. (Currently Amended) A semiconductor device comprising:

~~a semiconductor element~~ elements formed in a semiconductor

~~substrate, substrate;~~

a first interlayer insulation film formed over said semiconductor ~~element,~~  
elements; and

a first wirings, second wirings and third wirings formed ~~over-on~~ said first  
interlayer insulation film, respectively,

wherein said third ~~wiring is~~ wirings are electrically connected with said  
semiconductor ~~element~~ elements,

wherein said first and second wirings are not electrically connected with said  
semiconductor ~~element,~~ and elements,

wherein all of said first, second and third wirings are formed at a same layer,

wherein said second wirings are formed regularly, and

wherein each of said first wirings has a width larger than a width of each  
second wiring such that a planar size of said ~~each~~ first wiring is larger than a planar  
size of ~~said~~ each second wiring.

23. (Currently Amended) A semiconductor device according to claim 22,

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~~wherein said first, second and third wirings are formed at a same layer.~~further comprising:

a second interlayer insulation film formed on said first, second and third wirings; and

fourth wirings formed on said second interlayer insulation film and not electrically connected with said semiconductor elements,

wherein said fourth wirings are formed regularly.

24. (Currently Amended) A semiconductor device according to claim 22, wherein said first wirings and said second wirings are arranged in the row direction and/or column direction, respectively.

25. (Currently Amended) A semiconductor device according to claim 22, wherein said first wirings and said second wirings are ~~a dummy wiring~~wirings, respectively.

26. (Currently Amended) A semiconductor device according to claim 22, further comprising:

a second insulation film formed over said first interlayer insulation film and said first, second and third wirings,

wherein said second insulation film has an outer main surface that is substantially flattened.

27. (Previously Presented) A semiconductor device according to claim 22,

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wherein said first, second and third wirings are formed of aluminum or copper, respectively.

28. (Currently Amended) A semiconductor device comprising:  
a semiconductor element ~~elements~~ formed in a semiconductor substrate, ~~substrate~~;  
a first interlayer insulation film formed over said semiconductor element, ~~and elements~~; and  
~~a first and second dummy first wirings, second wirings and third wirings~~  
formed over ~~on~~ said first interlayer insulation film, respectively,  
wherein said third wirings are electrically connected with said semiconductor elements,  
wherein said first and second dummy wirings are not electrically connected with said semiconductor element, ~~and elements~~,  
wherein all of said first, second and third wirings are formed at a same layer,  
wherein said first wirings are formed regularly,  
wherein said second wirings are formed regularly, and  
wherein a planar size of said ~~each~~ first wiring is larger than a planar size of said ~~each~~ second wiring.

29. (New) A semiconductor device according to claim 28, wherein said first wirings and said second wirings are arranged in the row direction and/or column direction, respectively.

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30. (New) A semiconductor device according to claim 28, further comprising:

a second interlayer insulation film formed on said first, second and third wirings; and

fourth wirings formed on said second interlayer insulation film and not electrically connected with said semiconductor elements, wherein said fourth wirings are formed regularly.

31. (New) A semiconductor device comprising:

semiconductor elements formed in a semiconductor substrate:

a first interlayer insulation film formed over the semiconductor elements;

first wirings formed on the first interlayer insulation film and electrically connected with the semiconductor elements;

first dummy wirings and second dummy wirings formed on the first interlayer insulation film and not electrically connected with the semiconductor elements;

a second interlayer insulation film formed on the first wirings and on the first and second dummy wirings; and

third dummy wirings formed on the second interlayer insulation film and not electrically connected with said semiconductor elements,

wherein both the first dummy wirings and the second dummy wirings are formed at a same layer as the first wirings,

wherein each of the first dummy wirings has a width larger than a width of each second dummy wiring such that a planar size of each first dummy wiring is larger than a planar size of each second dummy wiring, and

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wherein the second dummy wirings and the third dummy wirings are formed regularly.